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Board Test

during

Design

and in

Production.

Hogeschool van Arnhem en Nijmegen
8 December 2011

Rob Staals, JTAG Technologies **robstaals@jtag.com**

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Why do we need to test?

Why do we need to test?

Simplified statement:

If the parts on a board are connected according to the design – the board should work.

Assumption:

Design is right
Components are OK

Conclusion:

Testing the interconnections should be sufficient to detect a great deal of bad boards.

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Test methods

- **Functional Test**
  Checks every function of the board (interconnects are implicitly tested)

- **Structural Test**
  Checks the structure of the board (i.e. interconnects, device orientation, device values etc.)

Functional Test

+ Excellent as an at-speed test
- However, what if the core of your board is not working
- You have to write/debug these functional tests manually
- Difficult to predict testcoverage
- Hard to pinpoint the exact location of the failure
- Requires highly trained (expensive) engineers
- Time consuming and costly

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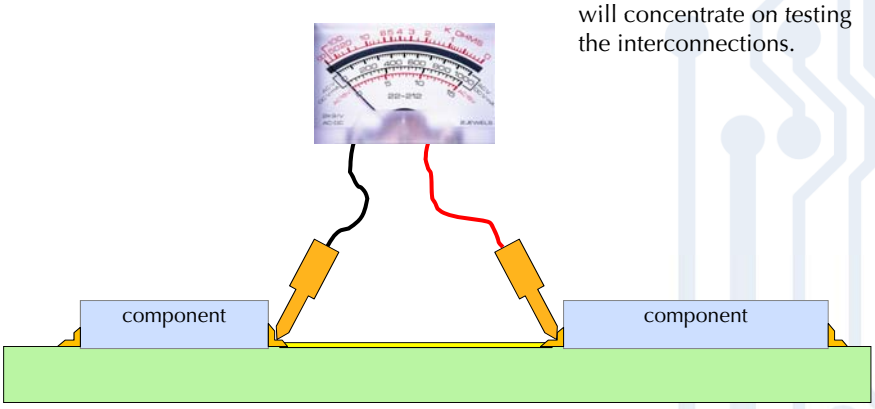
Structural Test

During this presentation we will concentrate on testing the interconnections.



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Structural Test

+ Assures the **Designer** that the interconnections on the board are according to the design. He/she no longer has to search for bad connections and can now fully concentrate on the design
+ Firmware independent
+ Automatic generation (based on Netlist)
+ Predictable Testcoverage
+ Pinpoints to the exact location of the problem
  if sufficient test points are available
- Is not an at speed test
+ Fast and inexpensive test method, important in **Production**

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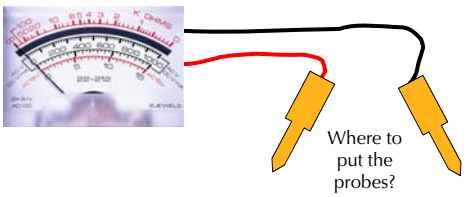
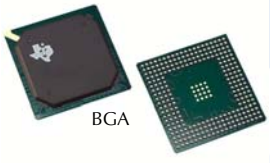
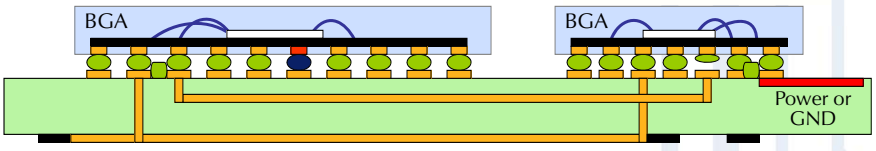
How to perform a Structural Test on a board using Hi-density devices



Where to put the probes?



BGA



The probes have no access to the Balls/Nets

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Solution to the access problem

Boundary-scan

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What is Boundary-scan

A Test method defined by the **Joint Test Action Group** (**JTAG**)

Officially approved in 1990

IEEE Std 1149.1 Standard Test Access Port and Boundary-Scan Architecture

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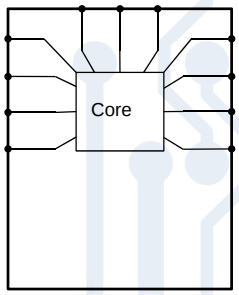
Principle of Boundary-scan

- Test logic integrated into the silicon of many standard chips (CPLDs, FPGAs, µC etc.)

  Suppliers such as:
  Altera, Xilinx, Atmel, Cypress, Lattice, Freescale, Infineon, NXP, TI, ST, etc. integrate 1149.1 into their devices.



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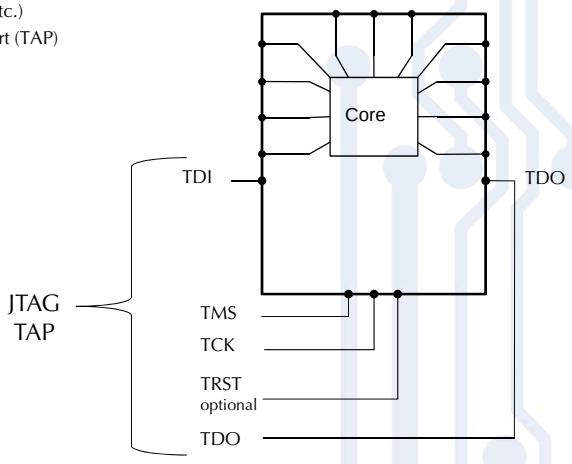
Principle of Boundary-scan

- Test logic integrated into the silicon of many standard chips (CPLDs, FPGAs, µC etc.)
- 4 (or 5) pins form the Test Access Port (TAP) or JTAG Interface
  TDI = Test Data IN
  TDO = Test Data Out
  TMS = Test Mode Select
  TCK = Test Clock
  TRST = Test Reset
  Optional



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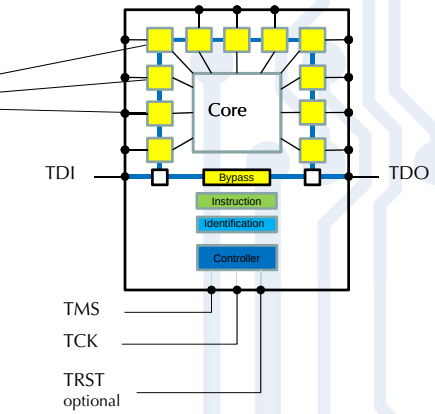

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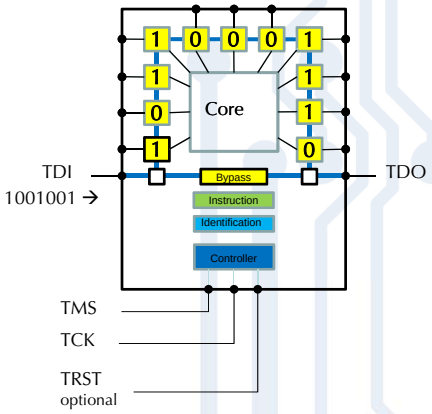
- Via TDI data can be shifted into the BSR or one of the other registers ……



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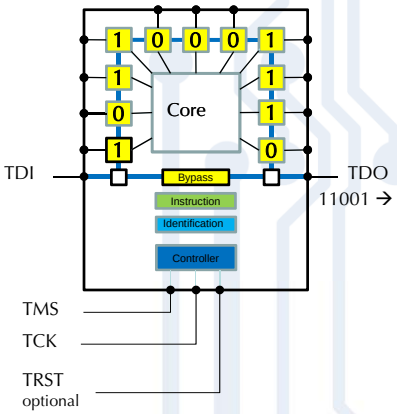
- … and shifted out via TDO



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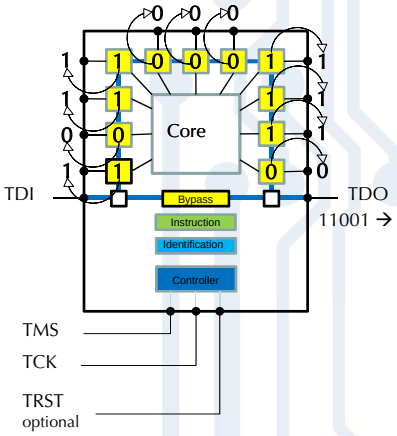
- … and shifted out via TDO

The instruction:

- Update puts the data from the Boundary-Scan Register (BSR) onto the pins. (drive)



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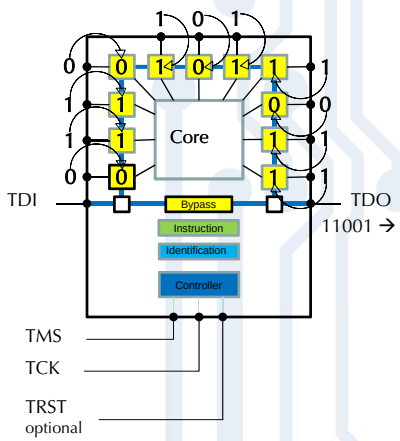
- … and shifted out via TDO

The instruction:

- **Update** puts the data from the BSR onto the pins. (drive)
- Capture reads the data from the pins and puts them into the BSR. (sense)



Each I/O pin can now be used for Driving and Sensing

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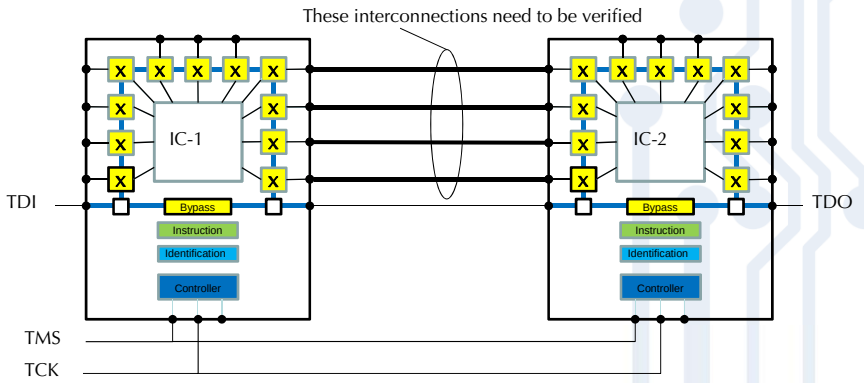
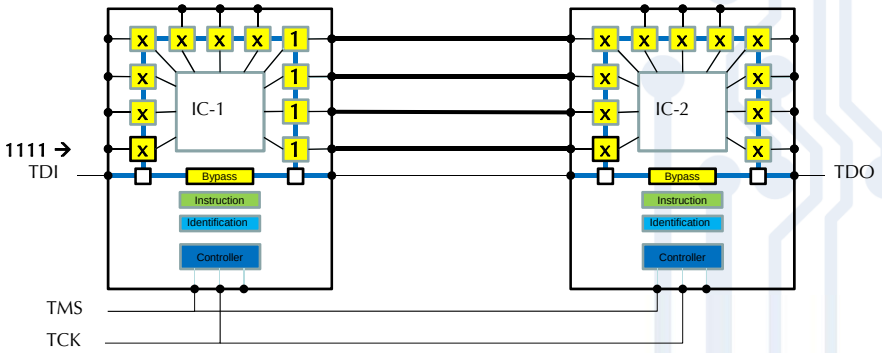
Example Interconnection Test



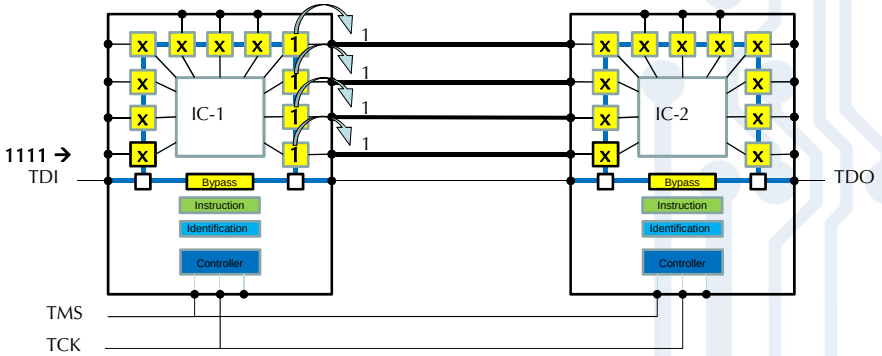
1. Put the BSRs from IC-1 and IC-2 in series, they form a Bscan chain

Example Interconnection Test



1. Put the BSRs from IC-1 and IC-2 in series, they form a Bscan chain
2. Shift testvector '..xxx1111xxx..' into the Bscan chain

Example Interconnection Test



1. Put the BSRs from IC-1 and IC-2 in series, they form a Bscan chain
2. Shift testvector '..xxx1111xxx..' into the Bscan chain
3. Update command drives the data from the Bscan chain onto the pins/nets

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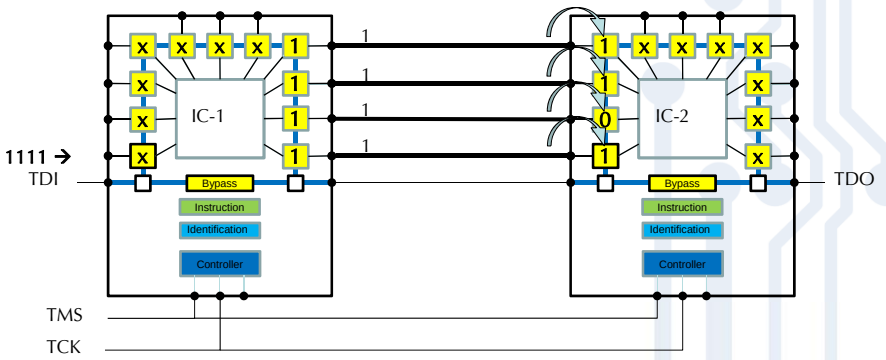
Example Interconnection Test



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2. Shift testvector '..xxx1111xxx..' into the Bscan chain
3. Update command drives the data from the Bscan chain onto the pins/nets
4. Capture command senses the data from the nets into the Bscan chain

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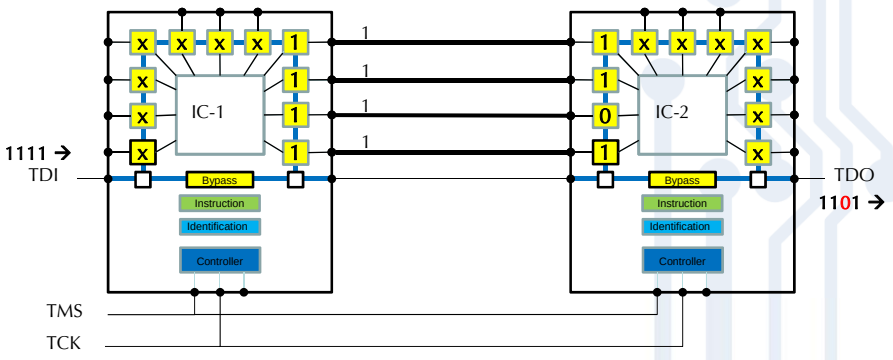
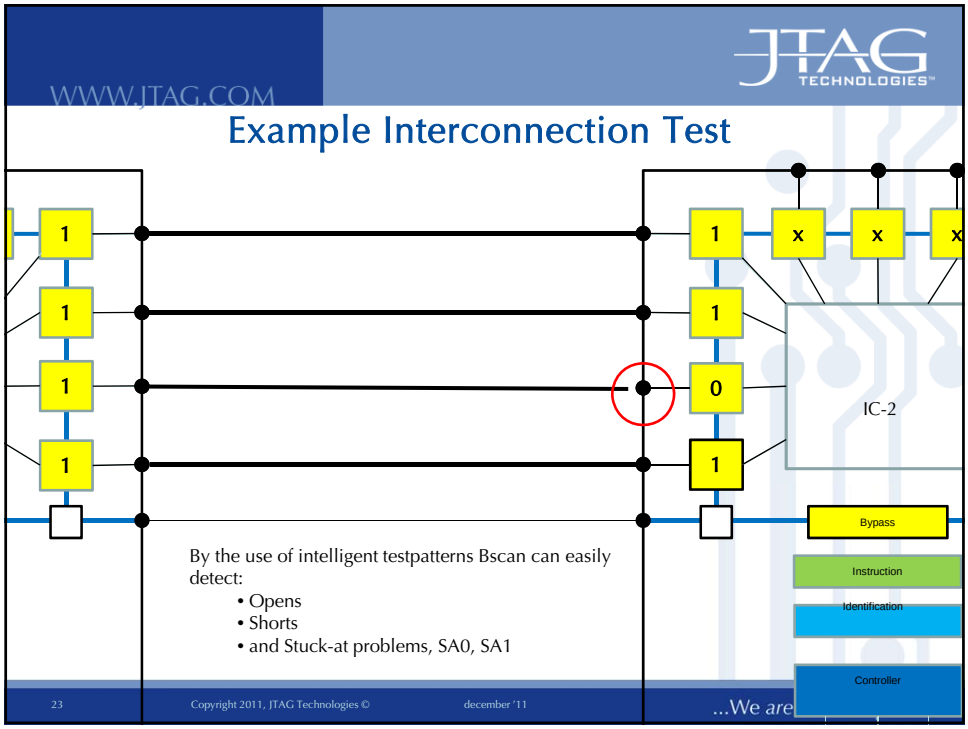
Example Interconnection Test



1. Put the BSRs from IC-1 and IC-2 in series, they form a Bscan chain
2. Shift testvector '..xxx1111xxx..' into the Bscan chain
3. Update command drives the data from the Bscan chain onto the pins/nets
4. Capture command senses the data from the nets into the Bscan chain
5. Shift captured vector out and compare with expected value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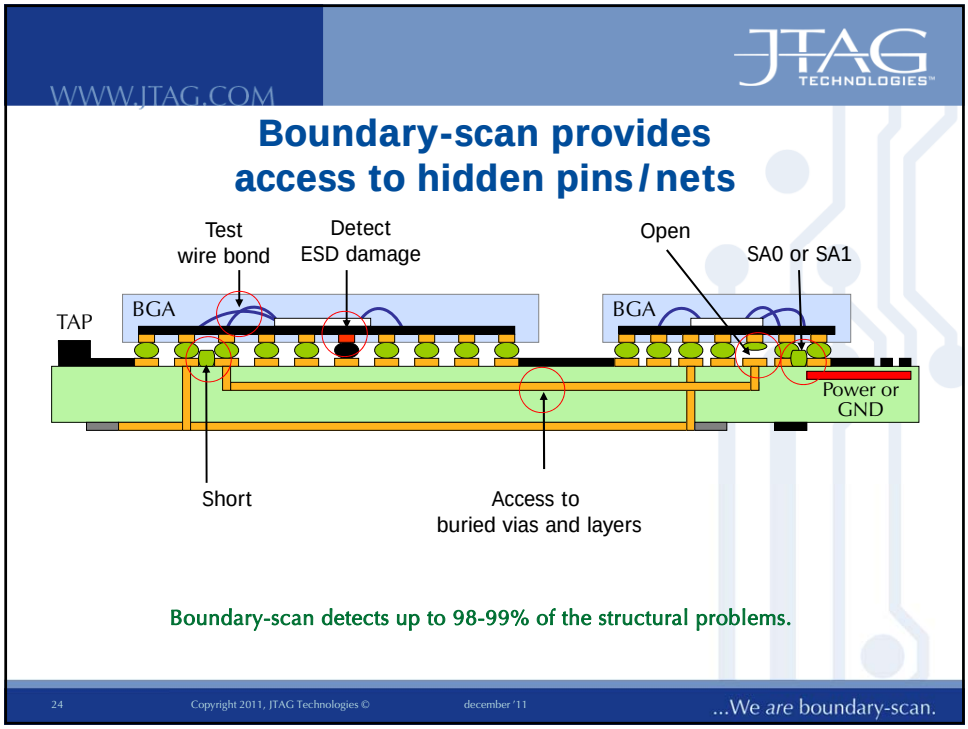
Example Interconnection Test
1
1
1
1
1
x
x
x
1
1
0
1
IC-2
Bypass
Instruction
Identification
Controller
By the use of intelligent testpatterns Bscan can easily detect:
• Opens
• Shorts
• and Stuck-at problems, SA0, SA1
23
Copyright 2011, JTAG Technologies ©
december '11
...We are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Boundary-scan provides access to hidden pins / nets
Test wire bond
Detect ESD damage
Open
SA0 or SA1
TAP
BGA
BGA
Power or GND
Short
Access to buried vias and layers
Boundary-scan detects up to 98-99% of the structural problems.
24
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...We are boundary-scan.

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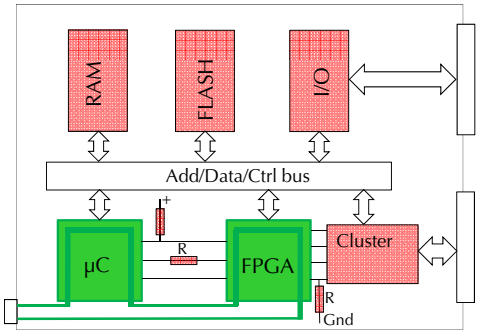
EXAMPLE µController board



This µController board contains 2 Bscan components (green) and the rest are non-Bscan devices such as Memory, Flash, Resistors, I/O, Connectors etc. (red)
What can you do with Boundary-scan?

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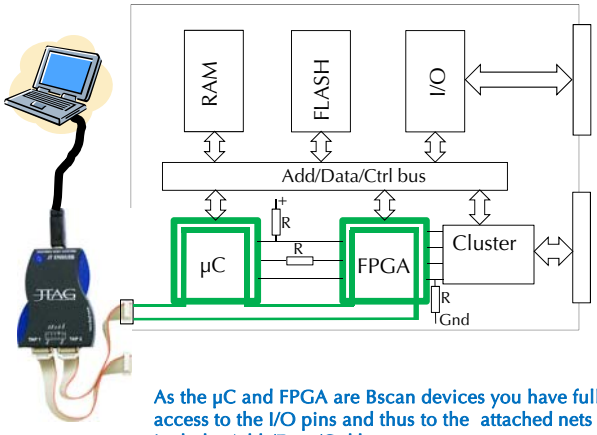
Connect a Bscan controller to the board



As the µC and FPGA are Bscan devices you have full access to the I/O pins and thus to the attached nets incl. the Addr/Data/Ctrl bus.

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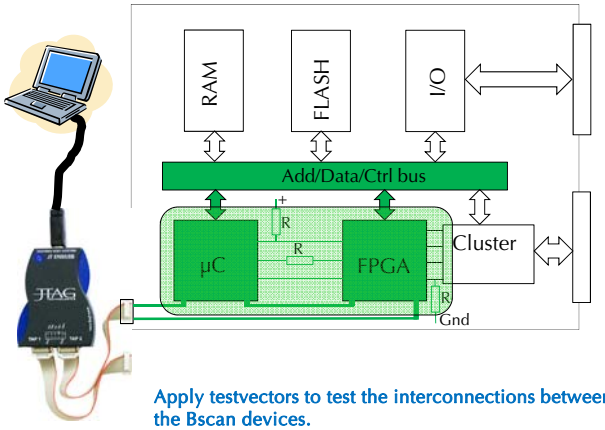
Interconnections Test



Apply testvectors to test the interconnections between the Bscan devices.

The Interconnection Test checks if the Bscan devices are correctly soldered onto the board.

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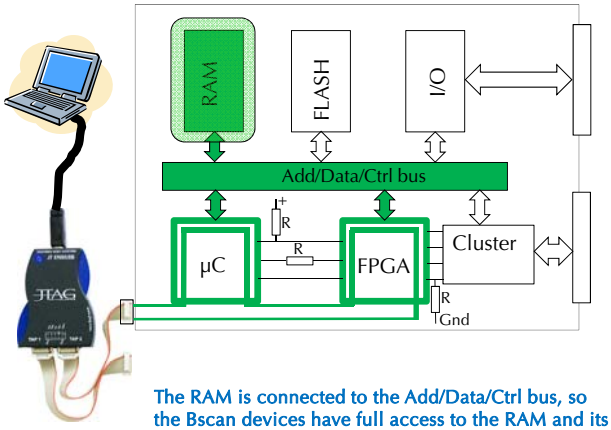
Memory Test



The RAM is connected to the Add/Data/Ctrl bus, so the Bscan devices have full access to the RAM and its connectivity can be tested.

All types of Static and Dynamic RAMs are supported incl. DDRs

The Memory Test checks if the device is correctly soldered onto the board.

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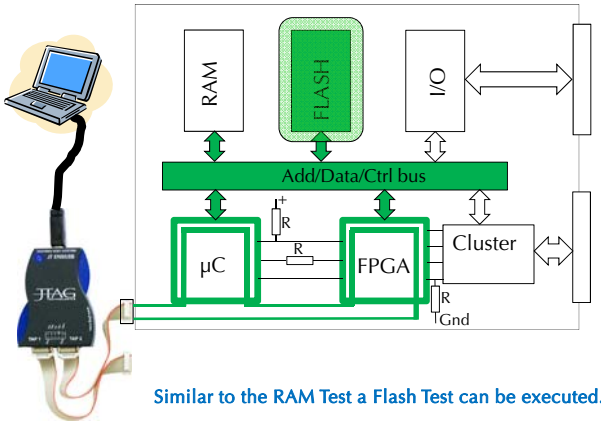
Flash Test



Similar to the RAM Test a Flash Test can be executed.

The Flash test contains:
-Verify ID code
-Blank check,
-Address bus test
-Data bus test

The Flash Test checks if the device is correctly soldered onto the board.

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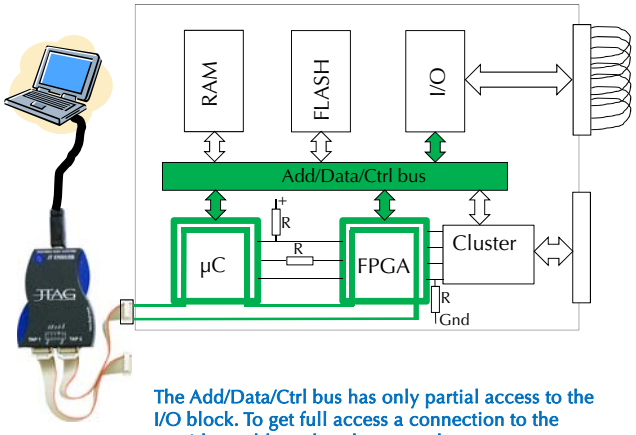
I/O Test



The Add/Data/Ctrl bus has only partial access to the I/O block. To get full access a connection to the outside world needs to be created.

A loopback connector could be used, however this does not always give you full access.

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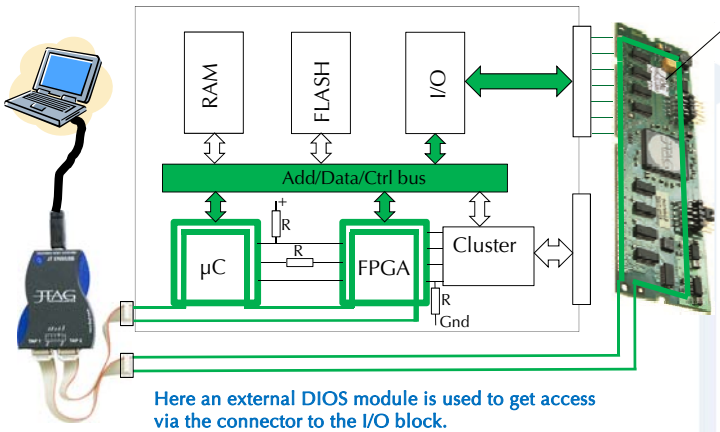
I/O Test



Here an external DIOS module is used to get access via the connector to the I/O block.

The DIOS module can be seen as a Boundary-scan device with a large number of I/O pins.

Access to the DIOS I/O pins is obtained through the JTAG interface.

In this case is the DIOS module connected to the second controller TAP, however it can also be cascaded with the first TAP.

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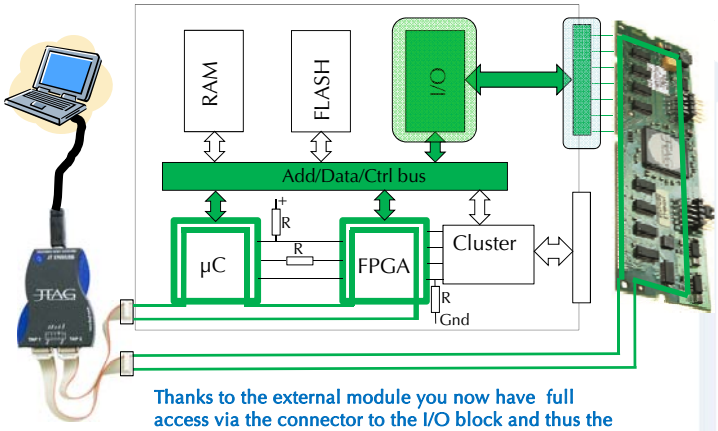
I/O Test



Thanks to the external module you now have full access via the connector to the I/O block and thus the connectivity of both can be tested.

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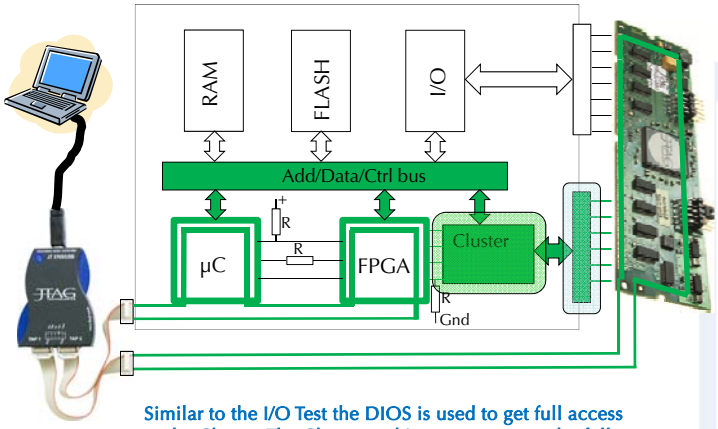
Cluster Test



The Cluster may contain all kind of logic i.e. glue logic, mixed signal such as ADC and DAC, Codec etc.

Similar to the I/O Test the DIOS is used to get full access to the Cluster. The Cluster and its connector can be fully tested.

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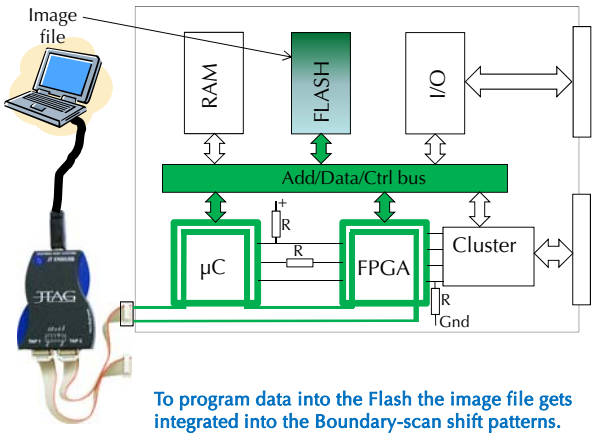
Flash Programming



Flash programming supports:
NAND and NOR type flashes with Parallel and Serial protocols (I2C, ISP etc.)

To program data into the Flash the image file gets integrated into the Boundary-scan shift patterns.

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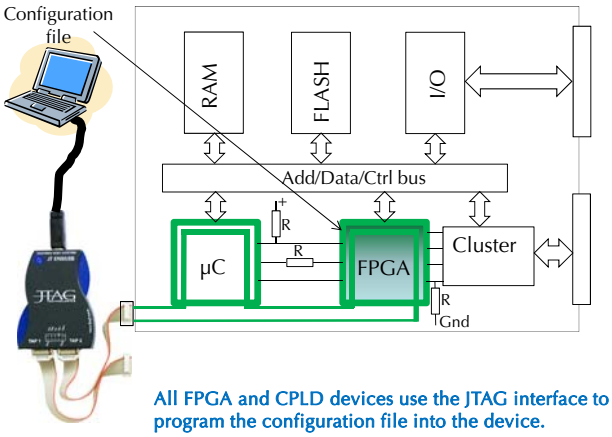
FPGA Programming



All FPGA and CPLD devices use the JTAG interface to program the configuration file into the device.

FPGA and CPLD devices from Altera, Xilinx, Lattice etc. use different file formats to configure their devices. (JEDEC, JAM,STAPL, SVF and IEEE1532).
All these formats are supported by our tools

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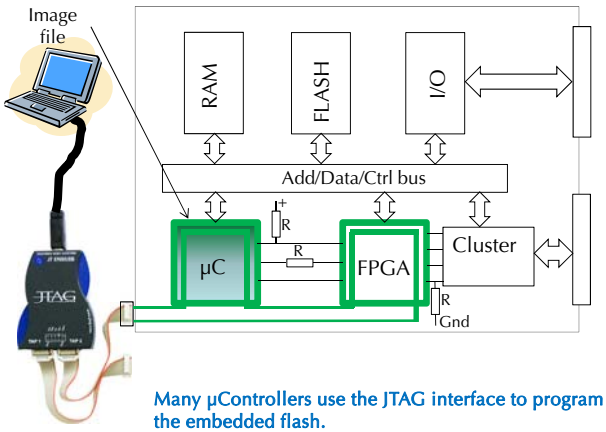
µC Programming



Many µControllers use the JTAG interface to program the embedded flash.

For most µControllers with embedded flashes we deliver dedicated programming solutions. (Atmel, Freescale, Infineon, NXP, Renesas, ST, TI etc)

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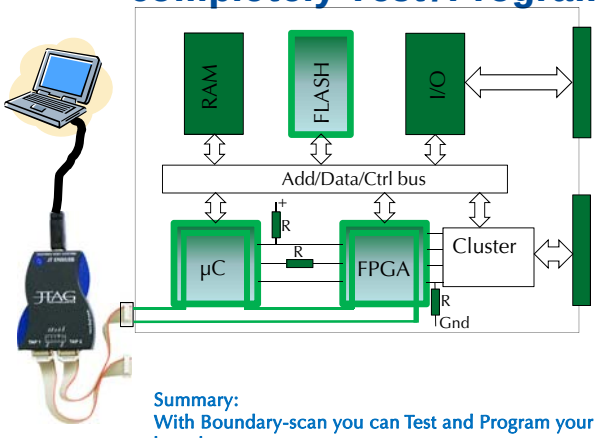
Boundary scan allows you to completely Test/Program the board



This example shows that with only a couple of Boundary-scan devices the complete board can be tested/programmed.

Summary:
With Boundary-scan you can Test and Program your board.

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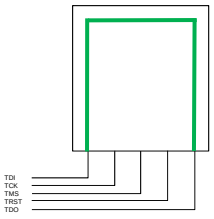
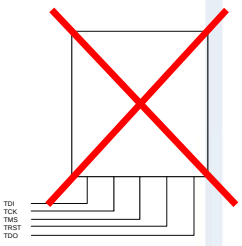
Important note

To implement the Boundary-scan architecture in your design at least one of the devices should comply to the IEEE1149.1 standard.
This means that the Bscan chain should be implemented in the device.



Bscan compliant



Not Bscan compliant

BSDL File

Real Boundary-scan devices come with a BSDL file

This file describes the behavior of the device in Bscan-mode
BSDL = Boundary Scan Description Language

BSDL files can be obtained from the device supplier

Example:

Altera: www.altera.com/download/board-layout-test/bsdl/bsdl.html
Xilinx: www.xilinx.com/isp/bsdl/bsdl.htm
Intel: downloadcenter.intel.com